REMARKS

Claims 1, 3-4, 7 and 9-11 are pending in this application, of which claims 1 and 11 have been amended. Claims 2, 5-6, 8 and 12 have been canceled. No new claims have been added.

Claims 1, 3, 4, 7 and 9-12 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite.

Accordingly, claims 1 and 11 have been amended to correct the noted instances of indefiniteness, and the 35 U.S.C. § 112, second paragraph, rejection should be withdrawn.

The Examiner has maintained the following prior art rejections from the previous Office Action:

1. The 35 U.S.C. § 103(a) rejection of claims 1, 3, 4, 7, 10 and 12 as unpatentable over **Liu et al.** in view of **APA**, **EP '623** and **Miller**; and
2. The 35 U.S.C. § 103(a) rejection of claims 9 and 11 as unpatentable over **EP '623** in view of **APA**.

Applicant respectfully traverses these rejections.

As noted in Applicant's previous response, **Lin et al.** discloses a method for electrolessly plating an overcoat metal on a metal conductor disposed on a dielectric surface of a substrate. The method includes removing carbonized film from the dielectric surface by applying a plasma discharge, acid treating the metal conductor by dipping the substrate in a first acid solution in order to clean the surface of the metal conductor, activating the metal conductor to allow electroless plating thereon by dipping the substrate in a metal activator solution, deactivating the

dielectric surface to prevent electroless plating thereon without deactivating the metal conductor by dipping the substrate in a second acid solution, and plating an overcoat metal on the metal conductor by dipping the substrate in an electroless plating solution so that the overcoat metal plates on and coats the metal conductor without plating on the dielectric surface.

The Examiner has admitted that the following features are not taught by **Liu et al.**:

1. The conductive pattern includes electrodes;
2. The space portion between the electrodes has a plurality of different dimensions;
3. That the oxidizing agent is coated selectively so that the oxidizing agent is formed selectively in portions, which are smaller than a predetermined dimension and the space portion, out of the space portion between the electrodes;
4. The ink jet application of the oxidizing agent; and
5. The space portion of less than 30 microns (claim 12).

The Examiner has cited **APA** for teaching that the conductive pattern includes electrodes, among other things.

EP ' 623 has been cited for teaching "that it is well known to overplate by electroless plating selectively over conductive patterns on a (Sic.) insulating substrate when making printed circuit boards, for example."

Miller has been cited for teaching an ink jet printing method including the step of applying materials for electroless plating in selective form.

None of the cited references teaches, mentions or suggests that the oxidizing agent is selectively coated in portions which are smaller than both a predetermined value and the distance between electrodes, where the distance between electrodes in the space portion between the electrodes has a plurality of different values, as in the present invention.

Accordingly, claim 1 has been amended to recite this distinction.

In particular, when a metal layer is selectively formed on the conductive pattern by electroless plating, because an electric short-circuit can easily occur in the narrow space portions (especially space portions smaller than 30 μm), the oxidizing agent or the protective film should be formed in the space portions in which the distance between electrodes is smaller than a predetermined distance where the electric short-circuit may easily occur.

None of the cited references teaches, mentions or suggests that it is easy to generate an electric short-circuit in the space portions which are less than a predetermined distance (smaller than 30 μm) in the electroless plating.

In fact, the specification discloses that it is difficult to form the solder resist pattern on space portions of the fine conductive patterns having a pitch of almost 60 μm or less.

That is, the phrase "the space portions which are smaller than 30 μm," now recited in claim 1 corresponds to minimum line width of the solder resist when the solder resist is patterned. Instead of patterning of the solder resist, this invention is applied so as to prevent electric short circuit between electrodes. In conventional technology, after the solder resist pattern is formed on the space portions between electrodes, electroless plating is applied while utilizing the solder resist pattern as a mask.

Accordingly, the limitation consisting of "the space portions which are smaller than 30 μm" is not taught or disclosed in **APA** or any of the other cited references.

In summary, it is not described in any of the cited references that when electroless plating is applied on the electrodes of the conductive pattern of the wiring substrate, the electrode which is connected to the connection pads of the electronic part, the oxidizing agent is selectively coated in the space portions which are smaller than 30 μm, thereby, the step of forming a solder resist pattern on the space portion is omitted.

Accordingly, claims 1 and 11 have been amended to clarify this distinction.

The Examiner has additionally cited U.S. Patent 5,549,808 to Farooq et al. (hereafter, "**Farooq et al.**") for teaching:

> Coating a protection film (resist 27) in spaces between a conductive pattern (see copper 18) such that the resulting protective film is selectively formed in a portion smaller than the spaces, allowing overplating that coats both the conductive traces and a portion of the space (see FIG. 13 and layer 23, for example).

Even if this is admitted, **Farooq et al.** fails to disclose the features recited in claims 1 and 11, as amended.

Thus, the 35 U.S.C. § 103(a) rejections should be withdrawn

In view of the aforementioned amendments and accompanying remarks, claims 1, 3-4, 7 and 9-11, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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